

In paragraph 1 of the Official Action, claims 16 - 23, 25, 27 - 29, and 40 were rejected under 35 USC 102(b) as anticipated by Fister et al (U.S. Patent No. 4,978,052, referred to below as Fister). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer. Independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer. Independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Fister does not disclose such products or such a method.

Fister discloses a system for attaching a semiconductor die to a substrate. In order to reduce thermal strains due to the mismatch between the coefficient of thermal expansion of a high conductivity substrate and a semiconductor die, a metallic buffer is disposed between the substrate and the die and is preferably sealed to the substrate by a layer of solder. The system of Fister nowhere involves forming a hot dip solder plating layer on an electroplated layer.

Figure 1 of Fister discloses an embodiment in which a solder preform 18 (see column 7, line 32) is disposed on a substrate 14 beneath a semiconductor die 12 and a buffer 16. There is no hot dip solder plating layer in this embodiment.

Figure 2 of Fister discloses an embodiment in which a layer of solder 18' is disposed between a buffer layer 16' having barrier layers 24 and 26 and oxidation resistant layers 20 and 22

on its top and bottom surfaces and a substrate 14' having a barrier layer 32 and an oxidation resistant layer 36 on its top surface. It is not described how the solder layer 18' is formed, but since it is illustrated as being an independent layer in the exploded view of Figure 2 (as opposed to the way in which plated solder layers 18" are illustrated in the exploded view of Figure 4), the solder layer 18' is clearly a preform, like the preform solder layer 18 of Figure 1. Thus, this embodiment lacks a hot dip solder plating layer on an electroplated layer.

Figure 4 of Fister illustrates an embodiment in which a solder layer 18" is hot dipped directly on both surfaces 28" and 30" of a buffer 16". There is no electroplated layer on which the solder layer 18" is formed, so this embodiment is also lacking a hot dip solder plating layer on an electroplated layer.

Figure 5 of Fister illustrates another embodiment in which a die 12''' is bonded to a substrate 14''' by a solder layer 18'''. There is no description of the structure of the solder layer 18''', but in light of the similarity between Figure 1 and Figure 5, the solder layer 18''' is clearly a preform, like solder layer 18 of Figure 1. Thus, this embodiment, too, does not have a hot dip solder plating layer on an electroplated layer.

Thus, contrary to the statements in the Official Action, nowhere in Fister is there any disclosure of forming a hot dip solder plating layer atop an electroplated layer, so Fister does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 17 - 23, 27 - 29, and 40 which depend therefrom. These claims are thus allowable.

The Official Action, referring to column 1, lines 49 - 58 of Fister, states that the method of Fister may be used to join a lid of a packaged part. Although this statement in the Official Action is not relevant to the claims rejected in this paragraph, the statement is nevertheless incorrect. Fister pertains solely to joining a semiconductor die to a substrate, and column 1, lines 49 - 58 is but background information, explaining that a sealed package in which a semiconductor is housed typically includes a lid. The method which Fister uses to join a semiconductor die to a substrate has nothing to do with how a lid is joined to a base of a semiconductor package. Column 8, lines 15 - 19 of Fister describe how a cap or lid 54 can be mounted on a leadframe 46, and this is by means of a glass seal produced by melting glass 50. Thus, Fister nowhere teaches that its method may be used to join a lid of a packaged part.

In paragraph 2 of the Official Action, claims 16 - 18, 20 - 22, 24, 25, 27, 28, 31, 34, 36, 39, 41, and 42 were rejected under 35 USC 102(b) as anticipated by Geschwind (U.S. Patent No. 4,331,258). This rejection is respectfully traversed.

As described above, independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath, while

independent claim 41 describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer.

Geschwind does not disclose such products or methods.

Geschwind discloses a sealing cover for a hermetically sealed container having a lid 12 made of an electrically resistant material, a metal plate "picture frame" on the circumference of one side and the edges of the lid, and a solder ring 16 adherent to and covering the picture frame. The solder ring may be formed by dip coating. Although it is disclosed that the picture frame may be created by selective metal plating, it is not disclosed in Geschwind which of various plating methods (electroplating, electroless plating, mechanical plating) is intended by Geschwind, and the term electroplating appears nowhere in the disclosure of Geschwind. Thus, Geschwind fails to disclose a hot dip solder plating layer on an electroplated layer, so it does not disclose all the features of claims 16, 20, 25, or 41 and cannot anticipate these claims or claims 17, 18, 21, 22, 27, 28, 31, 34, 36, or 42 which depend therefrom. These claims are thus allowable.

Claims 17, 21, and 27 further patentably distinguish the present invention from Geschwind. Claims 17, 21, and 27 recite an iron-nickel alloy as a material subjected to electroplating and then hot dip solder plating. Geschwind states in column 4, lines 12 - 15, "Of the metals/alloys in Table 1, the first eight are potentially acceptable as a material for the lid, while Invar, Kovar, and Alloy 42 do not possess the necessary

environmental resistance." Thus, Geschwind specifically rules out the use of a Fe-Ni alloy as a material for treatment and so does not anticipate claims 17, 21, or 27.

In paragraph 3 of the Official Action, claims 16 - 18, 20 - 22, 24, 25, 27 - 29, 31, 34, 36, 39, 41, and 42 were rejected under 35 USC 102(b) as anticipated by Nagashima et al (U.S. Patent No. Re. 34,484, referred to below as Nagashima). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer with a thickness of 10 - 50 μm on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer with a thickness of 10 - 50 μm on an electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath to form a hot dip solder plating layer with a thickness of 10 - 50 μm . Independent claim 41 describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer. Nagashima does not disclose any of these products or methods.

Nagashima describes gold-plated electronic components in which a plated layer of an alloy of nickel and cobalt is applied to a metal surface as an undercoat, and then a gold plated layer is formed atop the undercoat. Thus, the products disclosed by Nagashima are not solder coated materials at all but are gold-

plated members each having gold as its outermost layer.

Column 4, lines 29 - 33 of Nagashima describes a solderability test according to MIL STD 883-2003 in which leads of undisclosed structure are subjected to dipping in solder in order to test the wettability of the material to solder. This is no more than a test, and Nagashima nowhere discloses a product in which an electroplated layer has a hot dip solder plating layer. Furthermore, Nagashima contains no disclosure of the thickness of the solder resulting from hot dipping. The Official Action, referring to column 4, lines 17 - 20 of Nagashima, states that the solder in the soldering test has a thickness of about 50 μ m. However, the value of 50 μ m in column 4, lines 17 - 20 refers to the thickness of a solder preform ("A 1.0 t Kovar cap ... was sealed in a hydrogen furnace at 300° C. for 6 minutes using a 50 μ thick 80Au/20Sn preform") and has no relationship or relevance to the solderability test described in column 4, lines 29 - 33 of Nagashima.

Thus, Nagashima does not disclose a hot dip plating layer having a thickness of 10 - 50 μ m as set forth in claims 16, 20, 25, so it cannot anticipate these claims or claims 17, 18, 21, 22, 24, 27 - 29, 31, 34, 36, and 39 which depend therefrom.

With respect to claim 41, which describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer, the only method of forming a lid which is described in Nagashima is that set forth in the above-mentioned passage in column 4, lines 17 - 20, which method employs a solder

preform and is in no way related to a lid having a hot dip solder plating layer. Thus, Nagashima fails to disclose all the features of claim 41 and cannot anticipate it or claim 42 which depends therefrom.

In paragraph 4 of the Official Action, claims 16 - 25, 27, 31, 33 - 36, and 38 - 42 were rejected under 35 USC 103(a) as unpatentable over Dale (U.S. Patent No. 3,883,946). This rejection is respectfully traversed.

As described above, independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath, and independent claim 41 describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer. Dale does not disclose or suggest any such products or methods.

Dale discloses a method of securing a semiconductor body to a substrate by pressure bonding. As described in column 3, line 13 of Dale, a malleable metal layer of soft solder is disposed between a semiconductor body and a substrate, and a pressure of 1 - 5 tons per square inch is applied at a temperature of 75 - 300°C. Dale states that coatings of various materials can be formed on the substrate or the semiconductor body opposing the

solder layer, but there is no disclosure or suggestion of any of the coatings being formed by electroplating. The only specific method of forming a coating which Dale describes is silk screening for the case in which a coating is formed on a ceramic (column 5, line 33). The word electroplating never even appears in Dale. As for the soft solder, in all the examples of Dale, the solder is in the form of a foil, but Dale mentions briefly in column 6, lines 46 - 51 that the solder can be applied as a coating by dip soldering. However, there is no mention of the dip coating being formed anywhere except directly on the substrate or semiconductor body. Namely, solder is not applied by dip coating to an electroplated layer.

The Official Action asserts that it would have been obvious to have formed a metal coating on a substrate by electroplating because electroplating is simple and reliable. The Official Action presents no evidence in support of this assertion but merely presents the statement as a given. The mere fact that a technique may have advantages is by itself an insufficient basis for asserting that it would be obvious to employ the technique, for by this standard, every expedient which has advantages would necessarily be obvious. In order to establish obviousness, the Official Action must show some motivation in the references being relied upon to modify a reference. This the Official Action has failed to do, so the rejection does not set forth a *prima facie* case of obviousness and is improper.

Even if Dale were to be modified as proposed by the Official Action to form a metal coating by electroplating, since Dale only

describes the possibility of dip coating of solder being performed directly on a substrate or a semiconductor body, providing Dale with an electroplated layer would still not result in a hot dip solder plating layer on an electroplated layer, as set forth in the claims. Thus, as Dale does not disclose or suggest a hot dip solder plating layer formed on an electroplated layer, it does not disclose or suggest all the features recited in independent claims 16, 20, 25, and 41, so it cannot render these claims obvious. Claims 16, 20, 25, and 41 and claims 17 - 19, 21 - 24, 27, 31, 33 - 36, 38 - 40, and 42 which depend therefrom are thus allowable.

The Official Action states that Dale teaches a plated layer of material having excellent solderability and a solder coating to join a lid of a packaged part. This statement is incorrect. Column 9, lines 64 - 67 of Dale mention in passing that one example of a device to which the method of Dale is applied has a glass wall 63 with a sealing ring 67 of Kovar for use in attachment of a case lid, but there is no mention of the structure of the lid or of how the lid is joined to the wall 63. The lid is in fact irrelevant to the method of Dale, which is concerned solely with how to join a semiconductor body to a substrate. Dale clearly does not teach a lid of a packaged part including a hot dip solder plating layer on an electroplated layer.

The Official Action also states that the soldered portion in Dale may be applied to module devices. Column 10, lines 46 - 55 of Dale describe an embodiment of a method of pressure bonding to

secure three transistor elements on a conductive pattern applied on a ceramic member, with the member being employed in the manufacture of a transmitting transistor module device. However, this description in Dale has no relevance to those claims of the present application (claims 33 and 38) which refer to a module, since these claims state that a portion to be soldered is a shield of a module, or that a difficult to solder material forms a part of a shield of a module, and there is no mention of a shield of a module anywhere in Dale.

In paragraph 5 of the Official Action, claims 32 and 37 were rejected under 35 USC 103(a) as unpatentable over Dale in view of Akiba et al (U.S. Patent No. 6,353,540, referred to below as Akiba). This rejection is respectfully traversed.

Claims 32 and 37 depend from claim 20 and claim 25, respectively, and state that a portion to be soldered of an electronic part of claim 20 is a battery terminal, and that the difficult to solder material of claim 25 forms part of a battery terminal, respectively. As acknowledged by the Official Action, Dale discloses nothing about battery terminals. The statement in the Official Action that Dale teaches a hot dip solder plating layer on an electroplated layer has already been traversed above with respect to the rejection set forth in paragraph 4 of the Official Action.

The Official Action relies upon Akiba as supposedly teaching "bonding of batteries including shields", but Akiba teaches nothing about batteries. Akiba pertains to a circuit board

having low EMI, and the various embodiments of Akiba are various structures for such a circuit board. Column 4, lines 4 - 10 of Akiba describe a personal computer, shown in Figure 33, as an example of an electronic apparatus using a low EMI circuit board according to the invention of Akiba, and line 8 states that the personal computer includes a battery pack. That is the sole mention of a battery anywhere in Akiba, so there is clearly no disclosure in Akiba of a battery terminal as set forth in claims 32 and 37.

The Official Action also states that Akiba teaches bonding of batteries with a thin metal plating layer to which solder is bonded, and that solder may be applied by hot dipping. This statement is incorrect. The only mention of dipping in Akiba is in column 35, line 65, which states that after surface conductor patterns were printed on a sintered circuit board surface using a conductor paste, a resistor (which column 34, lines 32 - 34 identify as a commercially available resistor paste comprising a mixture of ruthenium oxide (RuO_2) powder and glass powder) was applied to both ends of the circuit board by the dipping method. Thus, Akiba does not disclose dipping of solder, and there is also no disclosure of the dipping in Akiba being atop an electroplated layer. Accordingly, Akiba has no relationship to the claims of the present application.

Therefore, as neither Dale nor Akiba discloses a battery terminal as a portion to be soldered or as a difficult to solder material as set forth in claims 32 and 37, the references lack teachings which could be combined so as to result in an

arrangement having all the features set forth in claim 32 or all the steps set forth in the method of claim 37 and so cannot render these claims obvious. Claims 32 and 37 are therefore allowable.

In paragraph 6 of the Official Action, claims 16 - 31, 34 - 36, and 39 - 42 were rejected under 35 USC 103(a) as unpatentable over Lichtenberger (U.S. Patent No. 6,390,353) in view of Elliott (U.S. Patent No. 5,232,562). This rejection is respectfully traversed.

As described above, independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath, and independent claim 41 describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer. Neither Lichtenberger nor Elliott discloses or suggests such products or methods.

Lichtenberger discloses an integral solder and plated sealing cover lid. As acknowledged by the Official Action, Lichtenberger does not disclose a hot dip solder plating layer on an electroplated layer.

Elliott was relied upon as supposedly teaching a method of forming a solder coated material including electroplating a layer

of material having excellent solderability and then forming a dip solder plating layer atop the electroplated layer, but Elliott contains no such teaching. Elliott in fact has no relationship to electroplating. Elliott discloses an electrochemical reduction treatment which performs cleaning of metallic surfaces in preparation for soldering. A reduction treatment liquid is applied to a surface of a component, and then the component is passed through a solder wave in a soldering treatment. The reduction treatment liquid is a liquid which reduces a surface oxide layer to clean a metal surface of oxides. An example of a reduction treatment liquid given in column 2, line 3 of Elliott is a sodium borate solution. Electrochemical reduction is thus totally different in nature from electroplating; it does not form an electroplated layer but instead removes material from a surface on which it is performed. This is why, as pointed out in column 2, line 19 of Elliott, electrochemical reduction is sometimes known as reverse plating.

The Official Action asserts that column 1, lines 66 - 68 of Elliott disclose electroplated layers of Cu or Sn which are subjected to hot dip solder plating. This assertion is incorrect. The term electroplating never appears in Elliott. Column 1, lines 66 - 68 refer to electrochemical reduction of copper and tin-lead surfaces. There is no statement of how the copper or tin-lead surfaces were formed, and certainly no suggestion of them being formed by electroplating; it is merely stated that the surfaces were subjected to electrochemical reduction (not electroplating) in a sodium borate solution.

Thus, since neither Lichtenberger nor Elliott discloses or suggests forming a hot dip solder plating layer atop an electroplated layer, the references do not contain teachings that could be combined so as to result in all the features set forth in claims 16, 20, 25, or 41 and so cannot render these claims obvious. Claims 16, 20, 25, and 41 and claims 17 - 19, 21 - 24, 26 - 31, 34 - 36, 39 - 40, and 42 which depend therefrom are thus allowable.

In paragraph 7 of the Official Action, claims 26, 29, and 30 were rejected under 35 USC 103(a) as unpatentable over Fister in view of Elliott, and in paragraph 8, claims 26, 29, and 30 were rejected under 35 USC 103(a) as unpatentable over Geschwind in view of Elliott. These rejections are respectfully traversed.

Claims 26, 29, and 30 depend from claim 25, which describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. As set forth above in the discussion of the rejection of paragraph 1 of the Official Action, the method disclosed by Fister does not involve forming a hot dip solder plating layer on an electroplated layer. As set forth in the discussion of the rejection of paragraph 2 of the Official Action, Geschwind does not contain any disclosure of electroplating, so it fails to disclose forming a hot dip solder plating layer on an electroplated layer. Elliott was relied upon in the Official Action as supposedly teaching a method of forming a solder coated material including electroplating a layer of material having

excellent solderability and then forming a dip solder plating layer atop the electroplated layer, but as set forth at length in the discussion of paragraph 6 of the Official Action, Elliott has no connection to electroplating.

Thus, as none of the three cited references discloses or suggests passing a difficult to solder material having an electroplated layer through a molten solder bath, they lack teachings which could be combined to result in a method having all the steps recited in claim 25 and included in claims 26, 29, and 30 by their dependence from claim 25, so the proposed combination of references cannot render these claims obvious. Claims 26, 29, and 30 are therefore allowable.

With respect to claim 26, the Official Action states that in Elliott, molten solder is subjected to ultrasonic vibration. Column 5, line 30 does use the word "ultrasonic" to refer to a soldering method, but it is not used in connection with a molten solder bath. Column 4, lines 54 - 58 of Elliott state that in one embodiment, a vibrator vane 36 is positioned in a nozzle 30 for solder, but the vibration range is specified as being below ultrasonic frequencies. Thus, Elliott clearly does not disclose or suggest ultrasonic vibration as recited in claim 26 in connection with a molten solder bath.

New claims 43 - 52 describe additional features of the present invention. Each of new claims 43 - 52 is allowable as depending from one of claims 16 - 42. New dependent claims 49 - 52 describe a method of manufacturing a solder coated material

including forming an electroplated layer and a hot dip solder plating layer on one but not both of a top and a bottom side of a continuous plate. The only one of the above references which discloses plating of a continuous member is Lichtenberger, and the method of Lichtenberger requires forming an electroplated layer on both sides of a substrate (for example, layers 20 on both sides of substrate 18 in Figure 1 of Lichtenberger), so Lichtenberger is not relevant to these claims.

In light of the foregoing remarks, it is believed that the present application is in condition for allowance, and favorable consideration is respectfully requested.

Respectfully submitted,



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